

VERSION SHOWING THE CHANGES TO THE SPECIFICATION

Amend the specification as follows:

Page 5, lines 20-33:

Figure 1 illustrates an embodiment of a logic gate with a charging FET with a potential-free gate electrode. The logic gate chosen is embodied here as an inverter since the inverter as the simplest component can illustrate the advantages of the present invention the most clearly. Figure 1 shows the connection in series of two transistors 2 and 4 to form an inverter. In this case, the transistor 2 is the switching transistor and the transistor 4 is the charging transistor. In figure 1, the source electrode 6 of the switching FET 2 is grounded. The drain electrode is connected to the output 12 of the inverter. The gate electrode 10 of the switching transistor 2 forms the input of the inverter. The source and drain electrodes of the charging transistor 4 connect the output 12 of the inverter to the supply voltage electrode 8.

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The two electrodes 8, 12 are connected by a semiconductor layer 24. An insulator layer 26 is arranged above the semiconductor layer 24. The gate electrode 20 is arranged above the insulator layer 26 24. In this case, the region 4 essentially defines the charging transistor and the region 16 essentially defines the region of the capacitive coupling between the gate electrode 20 and the electrode 8. With the reference symbols illustrated, the section illustrates one possible implementation of the charging FET of the inverter circuit from figure 3. With a different assignment of the reference symbols, the section illustrated can also be applied to the inverter circuit from figure 2.

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It is furthermore clear that the present invention can also be applied to tristate logic gates. It is clear that the electrodes ~~terminals~~ 6 and 8 can also be interchanged.